INPUT Frequency 10 MHz, ±5 x 10⁻⁷ Level +7 dBm ±5 dB into 50 ohms OUTPUT Frequency 50 MHz Level +13 dBm ±2 dB into 50 ohms STABILITY Aging 1×10^{-6} first vear after 30 days operating, typical 5×10^{-7} second year, typical 3×10^{-7} per year thereafter, typical Phase Noise L(f), static, free-running 100 Hz -135 dBc/Hz 1 kHz -155 dBc/Hz 10 kHz -169 dBc/Hz 100 kHz -170 dBc/Hz **Temperature Stability** $\pm 5 \times 10^{-7}$ free-running from 0 to $\pm 50^{\circ}$ C, (Ref. +25°C) Harmonics < -30 dBc Sub-Harmonics ≤ -80 dBc **PLL Divider Products** ≤ -80 dBc **Non-Harmonic Spurious** ≤ -80 dBc, excluding power supply line related spurs Phase Lock Alarm TTL Locked: +3.5 VDC to +5.2 VDC (Hi) Out-of-Lock: +0.8 VDC max (Lo) Phase Lock Voltage Monitor Voltage monitor pin supplied MECHANICAL Dimensions 2 x 2 x 1.3" Connectors SMA(f) and solder pins on side

Packaging Nickel-plated machined aluminum case - CVPLO POWER REQUIREMENTS Warm-Up Power \leq 8 Watts for 5 minutes Total Power \leq 5 Watts at +25°C Supply Voltage +15 VDC ±5% ADJUSTMENT Loop BW Target Bandwidth: ≤ 10 Hz Type 2 Loop CRYSTAL Type 50 MHz SC-cut (low-g) Acceleration Sensitivity $\leq 5 \times 10^{-10}$ /g per axis, typical ENVIRONMENTAL **Operating Temperature** 0° to +50°C Storage Temperature -40° to +85°C OTHER Label Use conventional label with the following information: 501-26245 (Current Rev.) 50 MHz PL Citrine +15 VDC Serial # - Date Code Test Data Output Level Phase Noise, Static, Free-Running Temperature Stability, Free-Running Harmonics, Subs, Products, Spurious Power – Warm-up and Total Acceleration Sensitivity

