INPUT Frequency 5 MHz Level +13 dBm ±1 dB into 50 ohms **OUTPUT** Frequency 50 MHz Level +13 dBm ±2 dB into 50 ohms **STABILITY** Aging (free-running) 1 x 10⁻⁶ first year after 30 days operating, typical 5 x 10⁻⁷ second year, typical 3 x 10⁻⁷ per year thereafter, typical Phase Noise L(f), (free-running) 10 Hz -110 dBc/Hz -140 dBc/Hz 100 Hz 1 KHz -162 dBc/Hz 10 KHz -176 dBc/Hz -176 dBc/Hz 100 KHz **Temperature Stability** ±5 x 10⁻⁷ free-running from 0 to +50°C (Ref. +25°C) **Harmonics** -25 dBc **Sub-Harmonics** -80 dBc Spurious -80 dBc, excluding power supply line related spurs Phase Lock Alarm TTL Locked: +3.5 VDC to +5.2 VDC (Hi) Out-of-Lock: +0.8 VDC max (Lo) **Phase Lock Voltage Monitor** Voltage monitor pin supplied **MECHANICAL Dimensions** 4.40 x 4.00 x 1" Connectors RF Input/Output: SMA(f) Power, Monitoring: Feed Thru Terminals **GND: Ground Turret**

Mounting

Warm-Up Power

Supply Voltage

ADJUSTMENT

Loop BW

CRYSTAL

Type

OTHER

Design

Label

+15 VDC ±5%

Type 2 Loop

50 MHz SC-cut

Total Power

Threaded inserts on base, 6 places

POWER REQUIREMENTS

≤ 6 Watts at +25°C

≤ 9.5 Watts for 5 minutes

Target Bandwidth: ~300 Hz

Includes x5 and x2 multipliers on the front

end to multiply the 5 MHz reference input

optimized for best close-in phase noise

performance using a ULN reference.

Use conventional label with the

(Mark connectors with function)

- Phase Noise - free-running

- Power - Warm-up and Total

- Harmonics, PLL Products, Spurious

following information:

Serial # - Date Code

50 MHz PL ULN

- Output Level

+15 VDC

Test Data

501-28835 (Current Rev.)

to 50 MHz for phase locking to the

internal oscillator. Loop BW will be

	REV	DATE	REVISION RECORD	DWN	AUTH
Packaging Nickel-plated machined aluminum housing – J1PM	-	03-05-15	Initial Release	PAC	
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