		REV	DATE	REVISION RECORD	DWN	AUTH
INPUT	Connectors	-	02-27-17	Initial Release	PAC	
Frequency	RF Input/Output: SMA(f)					
10 MHz	Power, Monitoring: Feed Thru Terminals					
Level	GND: Ground Turret					
+7 dBm ±6 dB into 50 ohms	Packaging					
	Nickel-plated machined					
				J3P MXO Connections		
Frequency	aluminum housing – J3P			Connector Function		
8.95 GHz	Mounting			1 Supply Voltage 2 Ground, Case		
Level	Threaded inserts on base,			4 RF Output		
+13 dBm \pm 2 dB into 50 ohms	#2-56, 6 places			5 Phase Lock Voltage 6 Phase Lock Alarm		
STABILITY	POWER REQUIREMENTS			7 External Reference Input		
Aging (free-running)	Warm-Up Power					
1 x 10 ⁻⁶ first year	≤ 15.5 Watts for 5 minutes	1.00				
after 30 days operating, typical	Total Power	0.75	- 00	1 🛈	S	
5 x 10 ⁻⁷ second year, typical	≤ 12 Watts at +25°C		56			
3×10^{-7} per year thereafter, typical	Supply Voltage	0.44 ⁻ 0.25 ⁻	7	2 🛈		
Phase Noise L(f), typical, (free-running)	+15 VDC ±5%	0				
10 Hz -52 dBc/Hz	ADJUSTMENT			ی ا		٥
100 Hz -82 dBc/Hz	Loop BW		0 0.40 0.68 0.68	1.45	4.81	5.0 1
1 KHz -110 dBc/Hz	Target Bandwidth: ≤ 10 Hz		╓╓╤╴	A		
10 KHz -130 dBc/Hz	Type 2 Loop	4.00 ⁻ 3.915 ⁻		4+%		
	CRYSTAL	3.915	- K			
100 KHz -131 dBc/Hz 1 MHz -131 dBc/Hz	Туре					
	89.5 MHz SC-cut (x100)					
Temperature Stability	OTHER					
$\pm 5 \times 10^{-7}$ free-running from 0 to $\pm 50^{\circ}$ C	Label					
(Ref. +25°C)	Use conventional label with the					
Harmonics	following information:	2.000	-0		0	
-25 dBc	501-30684 (Current Rev.)	2.000				
Sub-Harmonics	8.95 GHz MXO-PLD					
-60 dBc	+15 VDC					
PLL Divider Products	Serial # - Date Code					
-60 dBc	(Mark connectors with function)					
Spurious	Test Data			hreaded Inserts, #2-56 places, 0.15" deep		
-80 dBc, excluding power	- Output Level	0.085	ı 🖌 🦷	F	6	
supply line related spurs	- Phase Noise – free-running	0	_ <u>0</u> \		ر ر	
Phase Lock Alarm	- Temperature Stability – free-running		0.085		270	φ.
TTL	- Harmonics, Subs, Products, Spurious		0.0		2.2	ŋ
Locked: +3.5 VDC to +5.2 VDC (Hi)	- Power – Warm-up and Total	—				
Out-of-Lock: +0.8 VDC max (Lo)	ľ			Wenzel Associates, In	IC.	
Phase Lock Voltage Monitor				Austin, Texas		
Voltage monitor pin supplied		Title:				ы р\ -
MECHAŇICAL		8.9	5 GHZ M	ultiplied Crystal Oscillato	or (MXO-	PLD)
Dimensions		P/N:		Rev: Date: Drawn	: Re	ef:
5.36 x 4 x 1"		50	01-30684	- 02-27-17		
		Tolerances		0.XX Dec: 0.XXX Dec: FSCM:		_
		(except as Dimension	noted) s are in inches	±0.030" ±0.010" 6282	21 Page 1 o	of 1