

REV	DATE	REVISION RECORD	DWN	AUTH
-	02-25-10	Initial Release	PAC	

INPUT

Frequency

10 MHz, $\pm 1 \times 10^{-7}$

Level

+7 dBm ± 5 dB into 50 ohms

OUTPUT

Frequency

100 MHz

Level

+13 dBm ± 2 dB into 50 ohms

STABILITY

Output Phase Noise L(f)

(Free-Running)

- 10 Hz -100 dBc/Hz
- 100 Hz -130 dBc/Hz
- 1 kHz -158 dBc/Hz
- 10 kHz -176 dBc/Hz
- 100 kHz -176 dBc/Hz

Aging

$\pm 1 \times 10^{-6}$ per year after 30 days operating, typical

Temperature Stability

$\pm 5 \times 10^{-7}$ free-running from 0 to +50°C, (Ref. +25°C)

Harmonics

-30 dBc

PLL Divider Products

-70 dBc

Non-Harmonic Spurious

-80 dBc, excluding power supply line related spurs

Phase Lock Alarm

TTL

Locked: +3.5 VDC to +5.2 VDC (Hi)

Out-of-Lock: +0.8 VDC max (Lo)

Phase Lock Voltage Monitor

Voltage monitor pin supplied

MECHANICAL

Dimensions

2.5 x 3.5 x 0.8"

Connectors

SMA(f)'s and solder pins on side
Feed-thru terminals for lock alarm, supply and phase lock voltage monitor

Packaging

Machined aluminum housing

Mounting

Through holes, 4 places
Threaded inserts on base, 4 places

POWER REQUIREMENTS

Supply Voltage

+15 VDC $\pm 5\%$

Warm-Up Power

8 Watts at start-up for 5 minutes at +25°C

Total Power

5 Watts at steady state +25°C

ADJUSTMENT

Loop BW

Target Bandwidth: < 10 Hz
Type 2 Loop

CRYSTAL

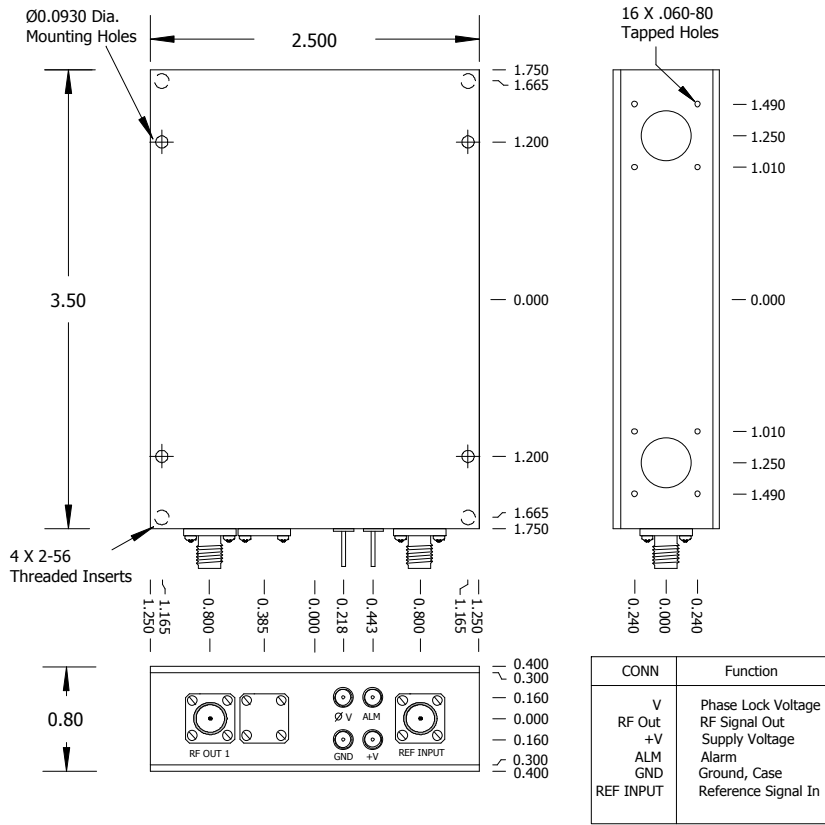
Type


100 MHz SC-cut

OTHER

Test Data

- Output Level
- Phase Noise (free-running)
- Temperature Stability (free-running)
- Harmonics, PLL Products, Spurious





Wenzel Associates, Inc.
Austin, Texas

Title: **100 MHz-SC ULN Phase Lock Crystal Oscillator**

P/N: 501-22114	Rev.: -	Date: 02-25-10	Drawn:	Ref:
Tolerances: (except as noted) Dimensions are in inches		0.XX Dec: ± 0.030"	0.XXX Dec: ± 0.010"	FSCM: 62821

Page 1 of 1